ABSTRACT

A novel and useful apparatus for and method of clock recovery from a serial data stream. The clock recovery mechanism of the present invention provides accurate and fast timing recovery while operative to filter out the effects of noise. The clock recovery mechanism clocks the received serial data into a shift register of N bits, where N is an even number equal to the oversampling factor of the data signal. A timing correction, generated during learning cycles, is applied during the subsequent correction cycle. The timing is adjusted during correction cycles by preloading the reference counter, from which the sampling clock is produced, such that its cycle is either shortened or extended by M clocks, where M corresponds to the required timing correction.